Nodari Sitchinava

Curriculum Vitae

University of Hawaii at Manoa
Department of Information and Computer Sciences
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https://algoparc.ics.hawaii.edu

Education

2009 Ph.D. (Computer Science), *University of California, Irvine*
Thesis: "Parallel external memory model and algorithms for multicore architectures"
Advisor: Michael T. Goodrich

2003 M.Eng. (Electrical Engineering and Computer Science), *Massachusetts Inst. of Technology*
Thesis: "Dynamic scan chains – a novel architecture to lower the cost of VLSI test"
Advisors: Rohit Kapur and Daniel A. Spielman

2002 S.B. (Electrical Engineering and Computer Science), *Massachusetts Inst. of Technology*

Professional Experience

University of Hawaii at Manoa — Honolulu, HI
Associate Professor — 2019 – current

University of Hawaii at Manoa — Honolulu, HI
Assistant Professor — 2014 – 2019

Karlsruhe Institute of Technology — Karlsruhe, GERMANY
Postdoctoral Researcher (Host: Prof. Peter Sanders) — Sept. 2011 – Dec. 2013

MADALGO, University of Aarhus — Aarhus, DENMARK
Postdoctoral Researcher (Host: Prof. Lars Arge) — Sept. 2009 – Sept. 2011

Synopsys, Inc. — Mountain View, CA
Research & Development Engineer in VLSI Test R&D Group — Sept. 2003 – Sept. 2004

Research Interests

Computational models for multicores and GPUs, parallel external memory and cache-oblivious algorithms, parallel data structures, energy-efficient computation, distributed processing of massive data

Teaching Experience

1. Lectures and Seminars

University of Hawaii at Manoa — 2019-2022
Graduate course "ICS 621: Analysis of Algorithms"
Taught in Fall 2019, Fall 2021, and Fall 2022

University of Hawaii at Manoa — 2014-2022
Undergraduate course "ICS 443: Parallel Algorithms"
Taught in Spring 2014, Fall 2017, and Spring 2022

University of Hawaii at Manoa 2014-2022
Graduate course "ICS 643: Advanced Parallel Algorithms"
Taught in Fall 2014, Fall 2016 and Spring 2022

University of Hawaii at Manoa 2015-2020
Undergraduate course "ICS 311: Algorithms"
Taught in Spring 2020, Spring 2019, Spring 2018, Spring 2017, Fall 2015, and Spring 2015

University of Hawaii at Manoa Fall 2018
Undergraduate course "ICS 491: Competitive Programming"

University of Hawaii at Manoa Spring 2016
Graduate course "ICS 691: Advanced Data Structures"

Karlsruhe Institute of Technology Winter 2012/2013
Graduate course "Algorithms for memory hierarchies"

Karlsruhe Institute of Technology Summer 2012
Seminar "Algorithms for realistic parallel models"

MADALGO, University of Aarhus Spring 2010
Graduate course "I/O-efficient graph algorithms" (together with Prof. Norbert Zeh and Dr. Deepak Ajwani)

MADALGO, University of Aarhus Summer 2008
Summer school on cache-oblivious algorithms (together with Professors Gerth Stølting Brodal, Erik Demaine and Norbert Zeh)

2. Invited Lectures

Guest Lecturer, Karlsruhe Institute of Technology Winter 2011/2012
"Algorithms II" by Prof. Peter Sanders.

Guest Lecturer, Karlsruhe Institute of Technology Winter 2011/2012
"Algorithms engineering" by Prof. Peter Sanders.

Guest Lecturer, MADALGO, Aarhus University Spring 2011
Graduate course "I/O algorithms" by Prof. Lars Arge.

Guest Lecturer, UC Irvine Spring 2008
Graduate course ICS 261 "Data structures" by Prof. David Eppstein.

Awards and Recognitions

Excellence in Teaching Award (nominated) 2021-2022
University of Hawaii at Manoa

Best paper award 2019
European Sympsium on Algorithms (ESA)

Publications *

1. Refereed Conference Publications

[C-1] P. Afshani, J. Iacono, V. Jayapaul, *B. Karsin*, N. Sitchinava. Locality-of-reference optimality of cache-oblivious algorithms. In *Proceedings of the Third SIAM Symposium on Algorithmic Principles of Computer Systems (APOCS)*, pages 31-45, **2022**.

[C-2] M.T. Goodrich, R. Jacob, N. Sitchinava. Atomic power in forks: a super-logarithmic lower bound for implementing butterfly networks in the Nonatomic Binary Fork-Join model. In *Proceedings of the 32nd ACM-SIAM Symposium on Discrete Algorithms (SODA)*, pages 2141-2153, **2021**.

[C-3] J. Ellert, J. Fischer, N. Sitchinava. LCP-aware parallel string sorting. In *Proceedings of the 26th International European Conference on Parallel and Distributed Computing (Euro-Par)*, pages 329-342, **2020**.

[C-4] *K. Berney*, N. Sitchinava. Engineering worst-case inputs for pairwise Merge Sort on GPUs. In *Proceedings of the 34th IEEE International Parallel & Distributed Processing Symposium (IPDPS)*, pages 1133-1142, **2020**.

[C-5] P. Afshani, R. Fagerberg, D. Hammer, R. Jacob, I. Kostitsyna, U. Meyer, M. Penschuck, N. Sitchinava. Fragile complexity of comparison-based algorithms. In *Proceedings of the 27th Annual European Symposium on Algorithms (ESA)*, pages 2:1-2:19, **2019**. **ESA Track A Best Paper Award**.

[C-6] * *B. Karsin*, V. Weichert, H. Casanova, J. Iacono, N. Sitchinava. Analysis-driven engineering of comparison-based sorting algorithms on GPUs. In *Proceedings of the 32nd ACM International Conference on Supercomputing (ICS)*, pages 86-95, **2018**.

[C-7] *K. Berney*, H. Casanova, *A. Higuchi*, *B. Karsin*, N. Sitchinava. Beyond binary search: parallel in-place construction of implicit search tree layouts In *Proceedings of the 32nd IEEE International Parallel & Distributed Processing Symposium (IPDPS)*, pages 1070-1079, **2018**.

[C-8] N. Sitchinava, D. Strash. Reconstructing generalized staircase polygons with uniform step length. In *Proceedings of the 25th International Symposium on Graph Drawing & Network Visualization (GD)*, pages 88-101, **2017**.

[C-9] R. Jacob, N. Sitchinava. Lower bounds in the Asymmetric External Memory model. In *Proceedings of the 29th ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)*, pages 247-254, **2017**.

[C-10] P. Afshani, M. deBerg, H. Casanova, *B. Karsin*, C. Lambrechts, N. Sitchinava, C. Tsirogiannis. An efficient algorithm for the 1D total visibility-index problem. In *Proceedings of the 19th Meeting on Algorithm Engineering & Experiments (ALENEX)*, pages 218-231, **2017**.

[C-11] * *B. Karsin*, H. Casanova, N. Sitchinava. Efficient batched predecessor search in shared memory on GPUs. In *Proceedings of the IEEE International Conference on High Performance Computing (HiPC)*, **2015**.

[C-12] P. Afshani, N. Sitchinava. Sorting and permuting without bank conflicts on GPUs. In *Proceedings of the 23rd European Symposium on Algorithms (ESA)*, pages 13-24, **2015**.

[C-13] R. Jacob, T. Lieber, N. Sitchinava. On the complexity of list ranking in the parallel external memory model. In *Proceedings of the 39th International Symposium on Mathematical Foundations of Computer Science (MFCS)*, pages 384-395, **2014**.

*As is customary in the respective communities, the authors of the publications at the algorithmic venues are listed alphabetically, while at the high-performance computing (HPC) ones are listed in the order of contributions. The latter are marked with an asterisk (*), with the main student contributor listed first and the advisor listed last. Italicized authors are current and former students of Nodari Sitchinava.

[C-14] P. Afshani, N. Sitchinava. I/O-efficient range minima queries. In *Proceedings of the 14th Scandinavian Symposium and Workshops on Algorithm Theory (SWAT)*, pages 1-12, **2014**.

[C-15] D. Ajwani, N. Sitchinava. Empirical evaluation of the parallel distribution sweeping framework on multicore architectures. In *Proceedings of the 21st European Symposium on Algorithms (ESA)*, pages 25-36, **2013**.

[C-16] M. Birn, V. Osipov, P. Sanders, C. Schulz, N. Sitchinava. Efficient parallel and external matching. In *Proceedings of the 19th International Conference Euro-Par 2013 Parallel Processing (Euro-Par)*, pages 659-670, **2013**.

[C-17] L. Arge, J. Fischer, P. Sanders, N. Sitchinava. On (dynamic) range minimum queries in external memory. In *Proceedings of the 13th International Symposium on Algorithms and Data Structures (WADS)*, pages 37-48, **2013**.

[C-18] N. Sitchinava, N. Zeh. A parallel buffer tree. In *Proceedings of the 24th ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)*, pages 214-223, **2012**.

[C-19] M.T. Goodrich, N. Sitchinava, Q. Zhang. Sorting, searching and simulation in the MapReduce framework. In *Proceedings of the 22nd International Symposium on Algorithms and Computation (ISAAC)*, pages 374-383, **2011**.

[C-20] D. Ajwani, N. Sitchinava, N. Zeh. I/O-optimal distribution sweeping on private-cache chip multiprocessors. In *Proceedings of the 26th IEEE International Parallel & Distributed Processing Symposium (IPDPS)*, pages 1114-1123, **2011**.

[C-21] D. Ajwani, N. Sitchinava, N. Zeh. Geometric algorithms for private-cache chip multiprocessors. In *Proceedings of the 18th European Symposium on Algorithms (ESA)*, pages 75-86, **2010**.

[C-22] L. Arge, M.T. Goodrich, N. Sitchinava. Parallel external memory graph algorithms. In *Proceedings of the 25th IEEE International Parallel & Distributed Processing Symposium (IPDPS)*, pages 1-11, **2010**.

[C-23] L. Arge, M.T. Goodrich, M. Nelson, N. Sitchinava. Fundamental parallel algorithms for private-cache chip multiprocessors. In *Proceedings of the 20th ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)*, pages 197-206, **2008**.

[C-24] D. Eppstein, M.T. Goodrich, N. Sitchinava. Guard placement for efficient point-in-polygon proofs. In *Proceedings of the 23rd Annual ACM Symposium on Computational Geometry (SoCG)*, pages 27-36, **2007**.

[C-25] * N. Sitchinava, S. Samaranayake, R. Kapur, E. Gizdarski, F. Neuveux, T.W. Williams. Changing scan enable during shift. In *Proceedings of the 22nd IEEE VLSI Test Symposium (VTS)*, pages 73-78, **2004**.

[C-26] * S. Samaranayake, E. Gizdarski, N. Sitchinava, F. Neuveux, R. Kapur, T.W. Williams. A reconfigurable shared scan-in architecture. In *Proceedings of the 21st IEEE VLSI Test Symposium (VTS)*, pages 9-14, **2003**.

2. Journal Publications

[J-1] *K. Berney*, H. Casanova, A. Higuchi, B. Karsin, N. Sitchinava: Beyond Binary Search: Parallel In-place Construction of Implicit Search Tree Layouts. *IEEE Transactions on Computers*, 71 (5): 1104-1116 (**2022**).

[J-2] N. Sitchinava and D. Strash. Reconstructing generalized staircase polygons with uniform step length. *Journal of Graph Algorithms and Applications*, 22 (3): 431-459 (**2018**).

[J-3] P. Afshani, M. deBerg, H. Casanova, *B. Karsin*, C. Lambrechts, N. Sitchinava, C. Tsirogiannis. An efficient algorithm for the 1D total visibility-index problem and its parallelization. *Journal of Experimental Algorithmics*, 23 (2): 2.3:1-2.3:23 (**2018**).

[J-4] F. Meyer auf der Heide, P. Sanders, N. Sitchinava. Introduction to the special issue on SPAA 2014. *ACM Transactions on Paralell Computing*, 3 (1): 1:1-1:2 (**2016**).

[J-5] N. Sitchinava. Computational geometry in the parallel external memory model. *SIGSPATIAL Special*, 4(2): 18-23 (**2012**).

[J-6] * S. Samaranayake, N. Sitchinava, R. Kapur, M. Amin, T.W. Williams. Dynamic Scan: driving down the cost of test. *IEEE Computer*, 35(10): 63-68 (**2002**).

3. Book Chapters

[B-1] M.T. Goodrich, N. Sitchinava. Parallel algorithms in geometry. In *Handbook of Discrete and Computational Geometry*. J.E. Goodman, J. O'Rourke, C.D. Tóth (editors), 3rd edition. CRC Press, 2017.

4. Refereed Workshops (without formal proceedings)

[W-1] N. Sitchinava, D. Strash. Reconstructing a unit-length orthogonally convex polygon from its visibility graph. *European Workshop on Computational Geometry (EuroCG)*, **2016**.

[W-2] R. Jacob, T. Lieber, N. Sitchinava. On the complexity of list ranking in the parallel external memory model. *Workshop on Massive Data Algorithmics (MASSIVE)*, **2015**.

[W-3] P. Afshani, N. Sitchinava. I/O-efficient range minima queries. *Workshop on Massive Data Algorithmics (MASSIVE)*, **2014**.

[W-4] N. Sitchinava, V. Weichert. Provably-efficient GPU algorithms. *Workshop on Massive Data Algorithmics (MASSIVE)*, **2013**.

[W-5] L. Arge, J. Fischer, P. Sanders, N. Sitchinava. On (dynamic) range minimum queries in external memory. *Workshop on Massive Data Algorithmics (MASSIVE)*, **2013**.

[W-6] D. Ajwani, N. Sitchinava, N. Zeh. I/O-optimal distribution sweeping on private-cache chip multiprocessors. *Workshop on Massive Data Algorithmics (MASSIVE)*, **2011**.

[W-7] D. Ajwani, N. Sitchinava, N. Zeh. Geometric algorithms for private-cache chip multiprocessors. *Workshop on Massive Data Algorithmics (MASSIVE)*, **2010**.

[W-8] L. Arge, M.T. Goodrich, N. Sitchinava. Parallel external memory model. *Workshop on Theory and Many-Cores (T&MC)*, **2009**.

[W-9] * N. Sitchinava, S. Samaranayake, R. Kapur, F. Neuveux, E. Gizdarski, T.W. Williams. Dynamically reconfigurable shared scan-in architecture. *IEEE International Test Synthesis Workshop (ITSW)*, **2004**.

[W-10] * N. Sitchinava, S. Samaranayake, R. Kapur, F. Neuveux, E. Gizdarski, T.W. Williams, D. Spielman. A segment identification algorithms for a dynamic scan architecture. *IEEE International Test Synthesis Workshop (ITSW)*, **2003**.

[W-11] * N. Sitchinava, S. Samaranayake, R. Kapur, M. Amin, T.W. Williams. DFT – ATE solution to lower the cost of test. *IEEE Workshop on Test Resource Partitioning*, **2001**.

5. Patents

[P-1] * R. Kapur, N. Sitchinava, S. Samaranayake, E. Gizdarski, F. Neuveux, S. Duggirala, T.W. Williams. Dynamically reconfigurable shared scan-in test architecture. US Patents 7900105, 7836368, 7836367, 7774663, 7743299, 7596733, 7418640.

Invited Presentations

1. Conference & Workshop Keynote Talks

[K-1] Workshop on Scientific Computing Carpentry March 22, 2013
Title: "Data locality in high-performance computing"

2. Selected Invited Talks

[T-1] Aarhus University (Host: Prof. Peyman Afshani) October 14, 2021
Title: "Atomic power in forks: a super-logarithmic lower bound for implementing butterfly networks in the nonatomic binary Fork-Join model"

[T-2] Lars Arge Memorial Symposium, Aarhus University October 10, 2021
Title: "Parallel buffer tree: advancing Lars Arge's legacy"

[T-3] Scalable Data Structures, Dagstuhl Seminar Series February 15, 2021
Title: "Atomic power in forks"

[T-4] Universitè Libre de Bruxelles (Host: John Iacono) June 27, 2018
Title: "Sorting in the Asymmetric External Memory model"

[T-5] Harvey Mudd College (Host: Ran Libeskind-Hadas) October 26, 2017
Title: "Sorting in the Asymmetric External Memory model"

[T-6] Technical University of Dortmund (Host: Prof. Johannes Fischer) July 28, 2017
Title: "Lower bounds in the AEM model"

[T-7] IIT – Madras (Host: Prof. John Augustine) December 14, 2015
Title: "Recent algorithmic advances in GPGPU computing"

[T-8] Algorithms Research Collaboration in Oresund Workshop (ARCO) November 27, 2015
Title: "Recent algorithmic advances in GPGPU computing"

[T-9] University of Münster (Host: Prof. Dr. Jan Vahrenhold) August 4, 2015
Title: "Locality-conscious Parallel Algorithms for Mobile Computing"

[T-10] 9th Scheduling for Large Systems Workshop July 1, 2014
Title: "Provably-efficient GPU algorithms"

[T-11] University of Chile (Host: Prof. Jérémy Barbay) November 27, 2013
Title: "(Dynamic) RMQ in the External Memory and Cache-oblivious models"

[T-12] Georgetown University (Host: Prof. Jeremy T. Fineman) November 14, 2013
Title: "Locality-conscious parallel algorithms"

[T-13] Stony Brook University (Host: Prof. Michael A. Bender) November 13, 2013
Title: "Locality-conscious parallel algorithms"

[T-14] ETH Zurich (Host: Dr. Riko Jacob) October 14, 2013
Title: "Parallel External Memory (PEM) model and its application to GPU computing"

[T-15] University of Kansas (Host: Prof. Joseph Evans) April 8, 2013
Title: "Data locality in high-performance computing"

[T-16] TU Eindhoven (Host: Prof. Mark de Berg) May 4, 2012
Title: "A parallel buffer tree"

[T-17] Georgia Institute of Technology (Host: Prof. David Bader) March 17, 2011
Title: "Parallel computing – a theoretical perspective"

[T-18] Goethe University Frankfurt (Host: Prof. Dr. Ulrich Meyer) December 20, 2010
Title: "Parallel computing – a theoretical perspective"

[T-19] University of California, Irvine (Host: Prof. Michael Goodrich) April 30, 2010
Title: "Geometric algorithms for private-cache chip multiprocessors"

[T-20] Cambridge University (Host: Prof. Simon Moore) April 22, 2009
Title: "Parallel external memory model for multicore architectures"

Grants

[G-1] PI, "AF: Small: Toward A Unified Model of Parallelism And Locality", National Science Foundation (NSF Grant 1911245), **$208,000**, 2019-2023.

[G-2] co-PI, "Cross-Scale Spatiotemporal Modeling Using an Integrated Data Framework", National Science Foundation (NSF Grant 1853866), **$349,999**, 2019-2022.

[G-3] PI, "Workshop on Parallel Algorithms and Data Structures", National Science Foundation (NSF Grant 1930579), **$37,094**, 2019-2020.

[G-4] PI, "AitF: FULL: Collaborative Research: Provably Efficient GPU Algorithms", National Science Foundation (NSF Grant 1533823), **$416,000**, 2015-2020.

[G-5] PI, "Hawaii Workshop on Parallel Algorithms and Data Structures", National Science Foundation (NSF Grant 1745331), **$40,346**, 2017-2018.

Leadership and Professional Service

Editorial Service

- **Guest Editor** for *ACM Transactions on Parallel Computing – Special Issue: Invited papers from SPAA 2014*

Program Committee Chairing and Organization

- **Chair & Organizer** of the *Second Hawaii Workshop on Parallel Algorithms and Data Structures*, 2019
- **Chair & Organizer** of the *First Hawaii Workshop on Parallel Algorithms and Data Structures*, 2017
- **Publicity Chair** for *ACM Symposium on Parallelism in Algorithms and Architectures*, 2015-2019
- **Chair** of the *Sixth Workshop on Massive Data Algorithmics (MASSIVE)*, 2014
- **Co-organizer** of the *24th Annual Symposium on Combinatorial Pattern Matching (CPM)*, 2013

Program Committees

- 35th ACM Symposium on Parallelism in Algorithms and Architectures (SPAA), 2023
- 34th ACM Symposium on Parallelism in Algorithms and Architectures (SPAA), 2022
- 29th IEEE International Conference on High-Performance Computing (HiPC), 2022
- 29th European Symposium on Algorithms (ESA - Track B), 2021
- 6th International Symposium on Algorithmic Aspects of Cloud Computing (ALGOCLOUD), 2020
- 32nd ACM Symposium on Parallelism in Algorithms and Architectures (SPAA), 2020
- 27th International Colloquium on Structural Information and Communication Complexity (SIROCCO), 2020
- 22nd SIAM Symposium on Algorithm Engineering & Experiments (ALENEX), 2020

- ◇ 30th ACM Symposium on Parallelism in Algorithms and Architectures (SPAA), 2018
- ◇ 20th Meeting on Algorithm Engineering & Experiments (ALENEX), 2018
- ◇ 31st IEEE International Parallel & Distributed Processing Symposium (IPDPS), 2017
- ◇ 23nd IEEE International Conference on High-Performance Computing (HiPC), 2016
- ◇ 24th European Symposium on Algorithms (ESA - Track B), 2016
- ◇ 15th Scandinavian Symposium and Workshops on Algorithm Theory (SWAT), 2016
- ◇ 30th IEEE International Parallel & Distributed Processing Symposium (IPDPS), 2016
- ◇ Eighth Workshop on Massive Data Algorithmics (MASSIVE), 2016
- ◇ 22nd IEEE International Conference on High-Performance Computing (HiPC), 2015
- ◇ Seventh Workshop on Massive Data Algorithmics (MASSIVE), 2015
- ◇ 26th ACM Symposium on Parallelism in Algorithms and Architectures (SPAA), 2014
- ◇ 16th Meeting on Algorithm Engineering & Experiments (ALENEX), 2014
- ◇ Fifth Workshop on Massive Data Algorithmics (MASSIVE), 2013

Student Clubs and Activities Advising

- ◇ *Faculty Advisor.* ACM Manoa Algorithms for Competitions and Interviews (PANDA) Club
- ◇ *Faculty Advisor and Coach for UH Manoa student teams.* ACM International Collegiate Programming Contest (ICPC), 2015, 2018, 2019

Community Outreach

- ◇ *Speaker.* Waipahu Intermediate School Career Day, Waipahu, HI, 2014-2016, 2018-2020
- ◇ *Speaker.* Leilehua High School Career Day, Wahiawa, HI, 2014, 2019